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2 Key features

2.1 ST802RT1A Ethernet PHY demonstration board

- ST802RT1A Fast Ethernet physical layer transceiver
- Onboard 3.3 V LDO regulator
- Onboard 25 MHz crystal
- 12 jumpers for boot-strap configuration (MII address, auto-negotiation, loopback, power-down, MII/RMII configuration)
- Several GND test points and jumpers for power consumption measurement
- Connectors
 - 20-pin full pitch header connector for debug purposes (compatible with the STM32F207 controller demonstration board)
 - RJ45 connector with embedded transformer
 - 40-pin connector footprint compatible with the Spirent® Communications SmartBits 200/2000 (SMB-200/SMB-2000) analysis system (connector is not assembled).

2.2 STM32F207 controller demonstration board

- STM32F207 Connectivity Line Cortex™-M3 based microcontroller with embedded Ethernet MAC
- Onboard 3.3 V LDO regulator
- Onboard 25 MHz crystal
- Reset button, power LED, general purpose button, and two LEDs
- Connectors
 - 20-pin full pitch header connector for debug purposes (compatible with the ST802RT1A demonstration board)
 - 20-pin JTAG connector
 - Additional general purpose 20-pin full pitch header connector
 - USB device connector (+5.0 V power supply).

3 General system description

The STEVAL-PCC010V2 ST802RT1A Ethernet PHY demonstration kit consists of two boards. The ST802RT1A demonstration board was designed for chip evaluation purposes and therefore allows the user to simply select the PHY boot options, to evaluate the power consumption of the chip, and to attach the device to the professional test equipment.

Additionally, the STM32F207 controller demonstration board extends the ST802RT1A demonstration board with an STM32™ F-2 series microcontroller and its embedded MAC. This allows to immediately start evaluation of an internet appliance based on the embedded microcontroller and the Ethernet PHY. By default, the controller demonstration board is pre-Flashed with a web server application for demonstration purposes.

Figure 3. ST802RT1A Ethernet PHY TX mode demonstration kit

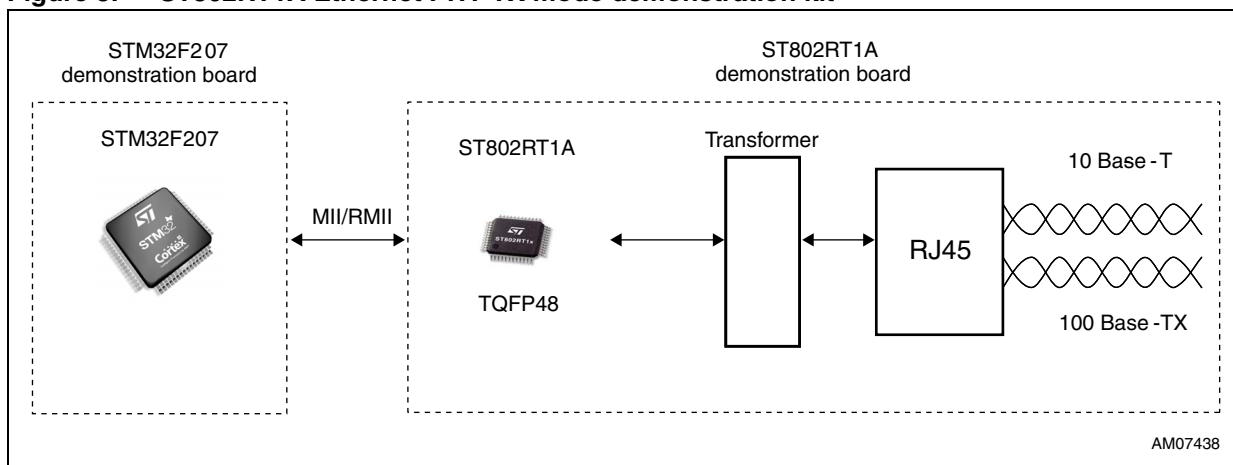


Figure 3 shows the ST802RT1A Ethernet PHY TX mode demonstration kit consisting of two boards: the ST802RT1A Ethernet PHY demonstration board and the STM32F207 controller demonstration board connected through the MII/RMII connector.

4 Getting started

This section briefly describes how to start using the STEVAL-PCC010V2, ST802RT1A Ethernet PHY TX mode demonstration kit. In order to use this demonstration kit a web browser must be installed on your PC.

4.1 Package contents

The ST802RT1A Ethernet PHY TX mode demonstration kit includes the following:

4.1.1 Hardware content

- One ST802RT1A Ethernet PHY demonstration board
- One STM32F207 controller demonstration board

4.1.2 Software content

- Web server - demonstration software based on lwIP TCP/IP stack

4.1.3 Documentation

- STM32 and ST802RT1A datasheets
- This user manual

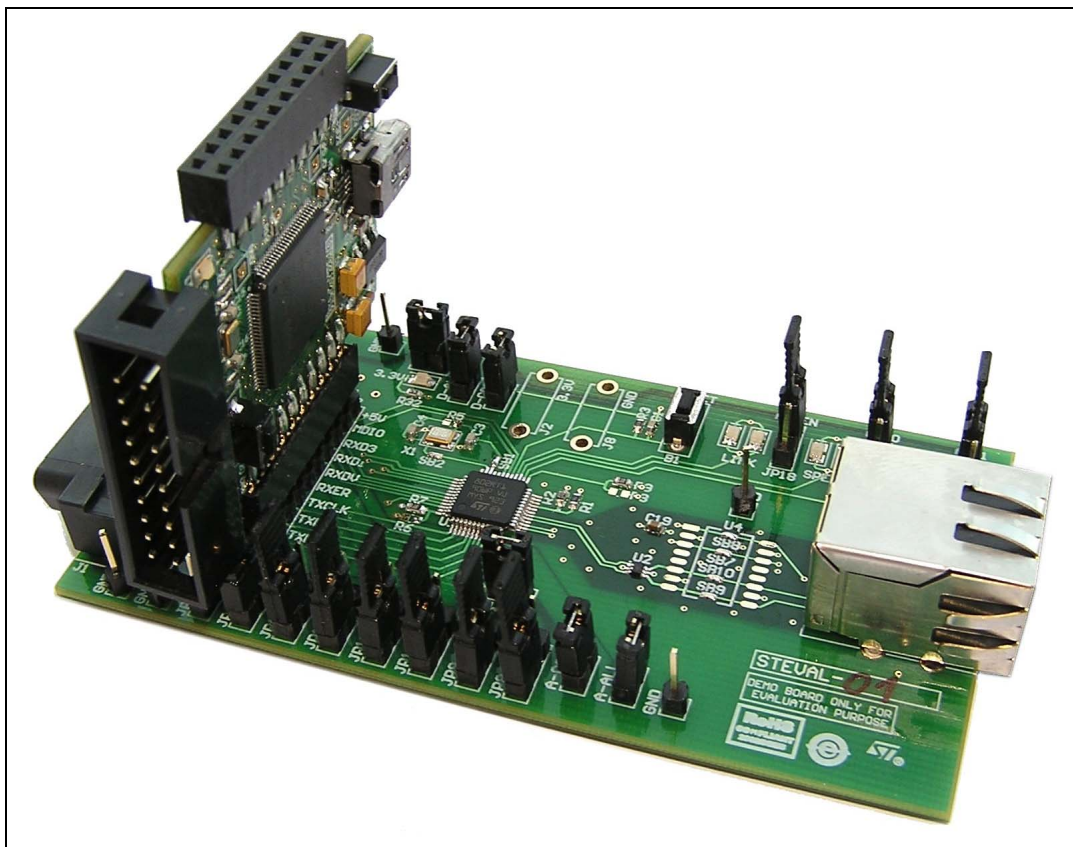
4.2 How to run the demonstration software

This section describes the demonstration software delivered with the ST802RT1A Ethernet PHY TX mode demonstration kit. The software implements a simple web server based on lwIP TCP/IP stack. The web server consists of three pages displaying some general information about STM32 and ST802RT1A, allowing to control LEDs on the STM32F207 controller demonstration board, and also shows the content of the ST802RT1A PHY registers.

To run the demonstration software one STEVAL-PCC010V2 demonstration kit, an Ethernet cable, and a PC with a web browser is required.

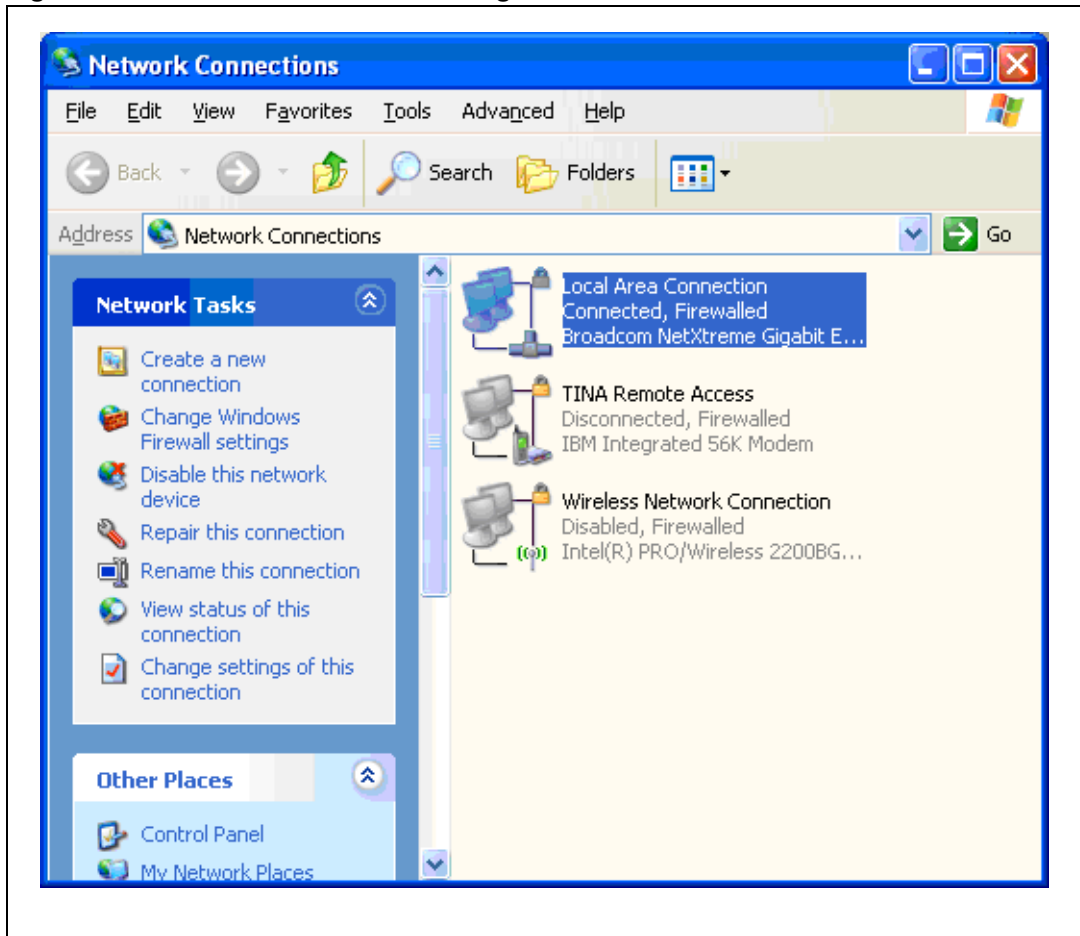
1. Connect boards delivered in the package as shown in [Figure 4](#):

Figure 4. ST802RT1A demonstration board connected to the STM32F207 demonstration board



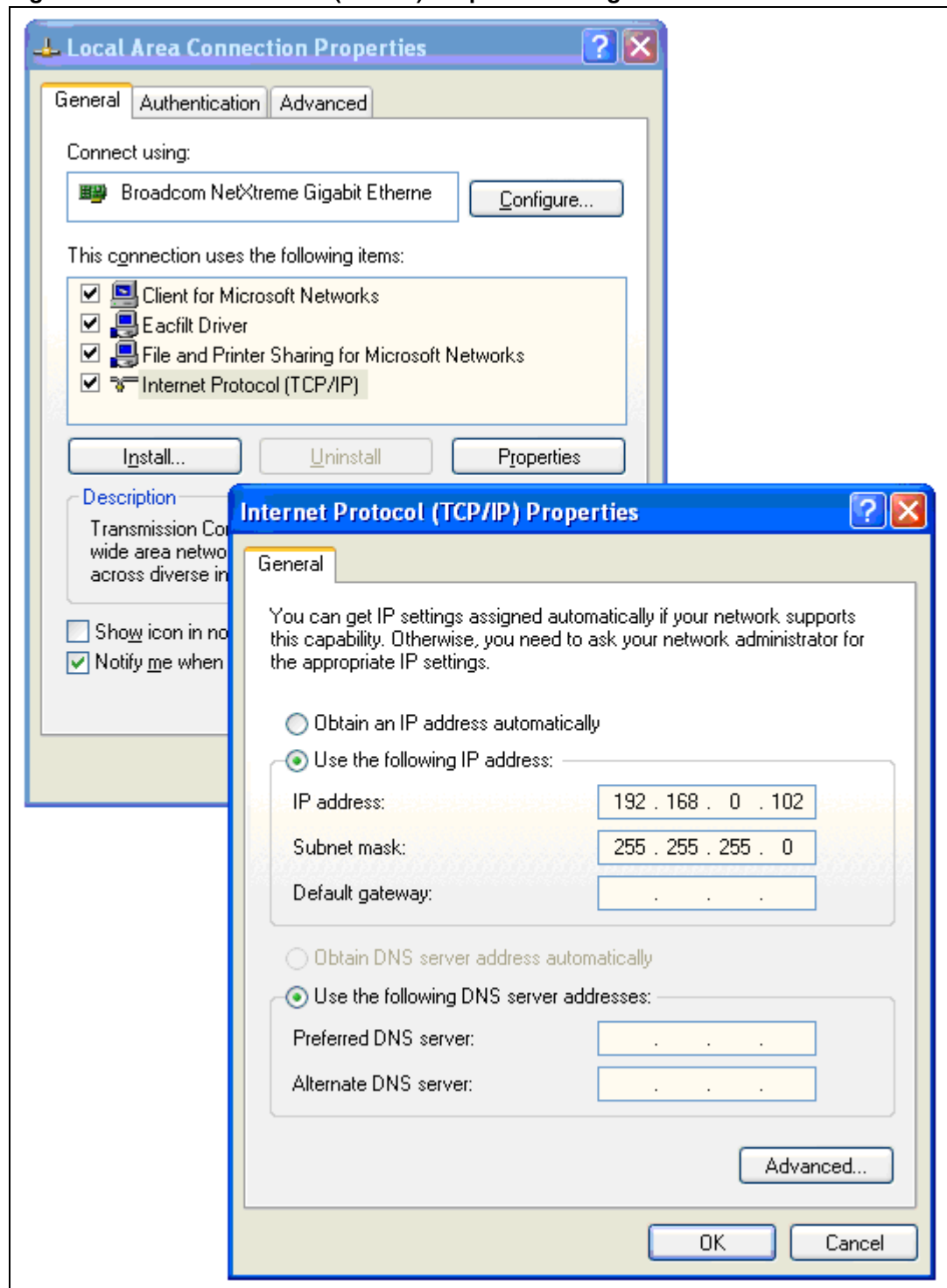
2. Set up the jumpers on the ST802RT1A Ethernet PHY demonstration board. The software does not change any settings of the PHY; it reads the settings from the PHY instead. See [Section 6.1](#) for more details of board setup.
3. Connect ST802RT1A Ethernet PHY board to the STM32F207 controller demonstration board.
4. Connect the Ethernet cable to the ST802RT1A Ethernet PHY board on one side and to the PC on the other side.
5. Flash the demonstration software into the Flash of the STM32F207 MCU.
6. Configure the PC. The following description is valid for Windows® XP; nevertheless it is easy to set up any other operating system in a similar way.
 - a) Set network settings: in control panel choose Network Connections, right click on the network card, and open Properties.

Figure 5. Network connections dialog box



- b) Select IP protocol properties: select Internet Protocol (TCP/IP) and click Properties.

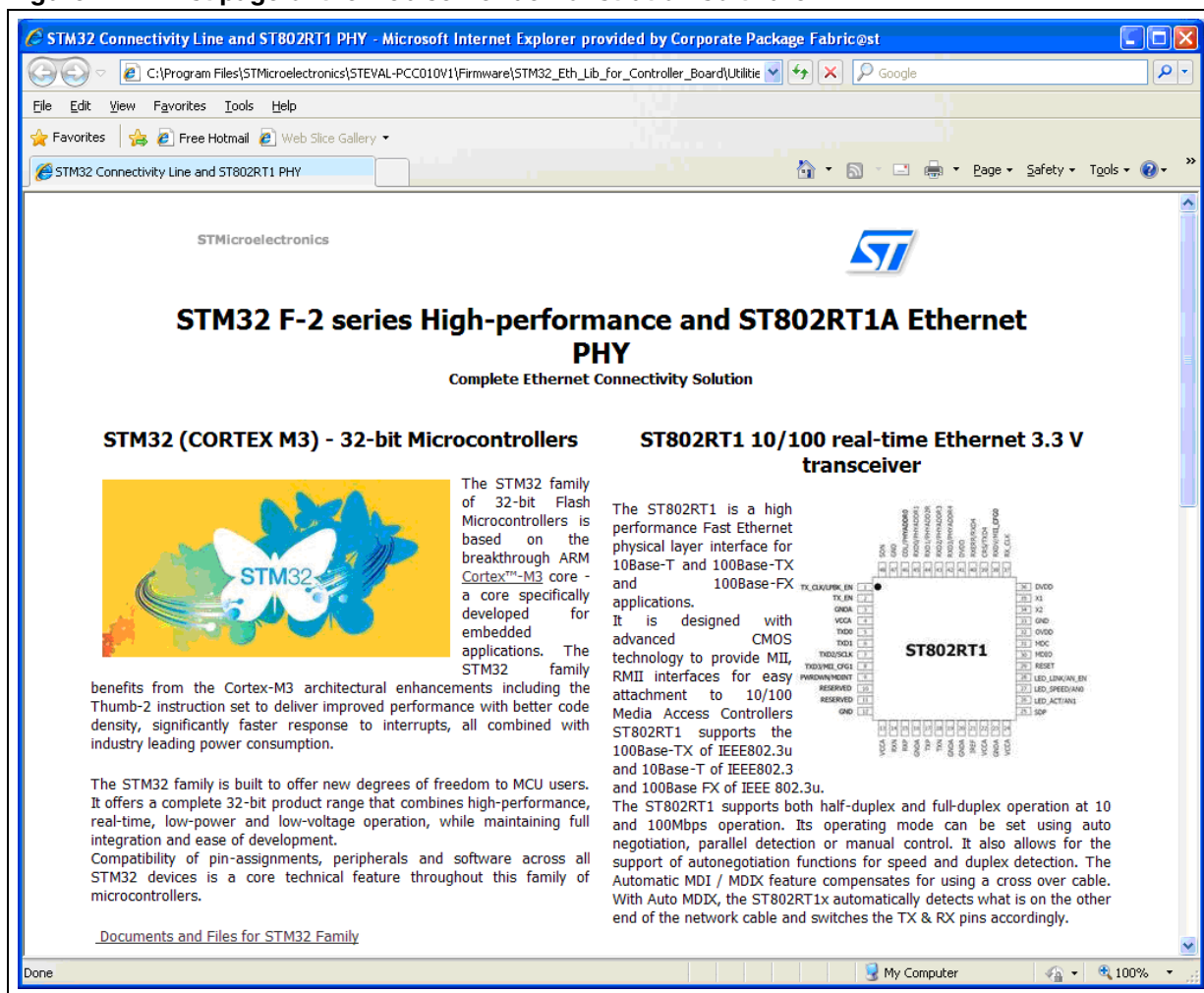
Figure 6. Internet Protocol (TCP/IP) Properties dialog box



- c) Change the IP settings to:
 - IP Address:** 192.168.0.4 (or any other different to 192.168.0.8, as in [Figure 6](#))
 - Subnet mask:** 255.255.255.0
- d) Disable firewall(s) running on the PC.

- 7. Run the web browser and open page <http://192.168.0.8>. It should be possible to see the first page of the web server running on the demonstration kit.

Figure 7. First page of the web server demonstration software

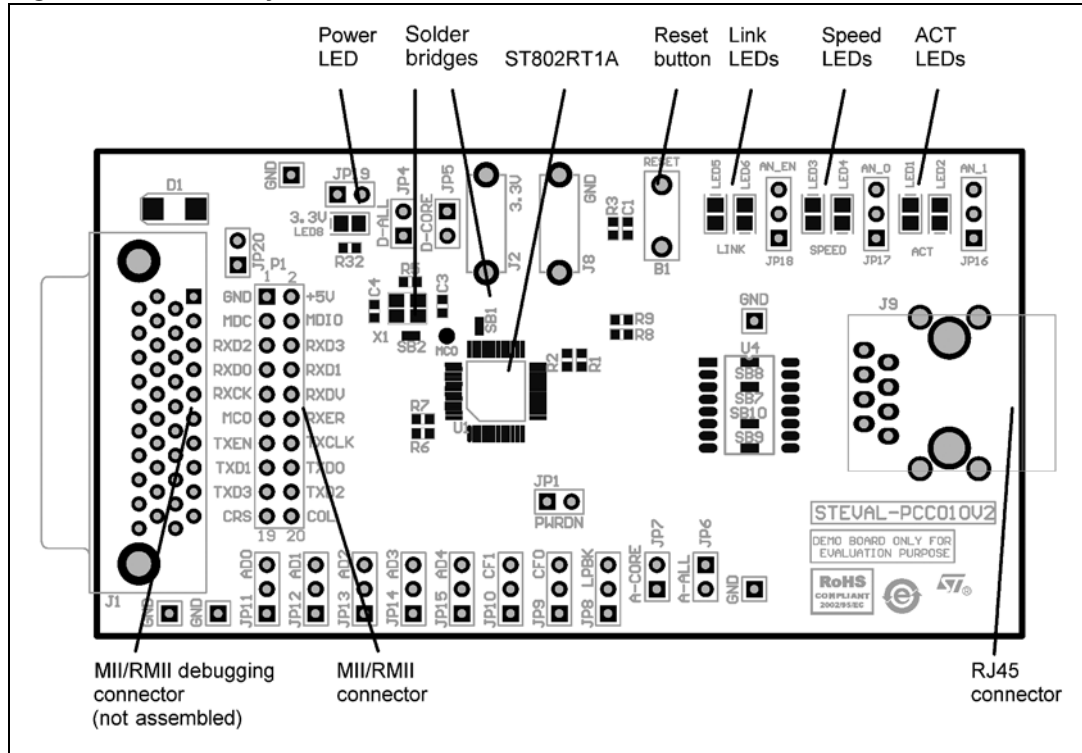


- 8. It is also possible to ping to the board using the ping command on your PC.

5 Board layout

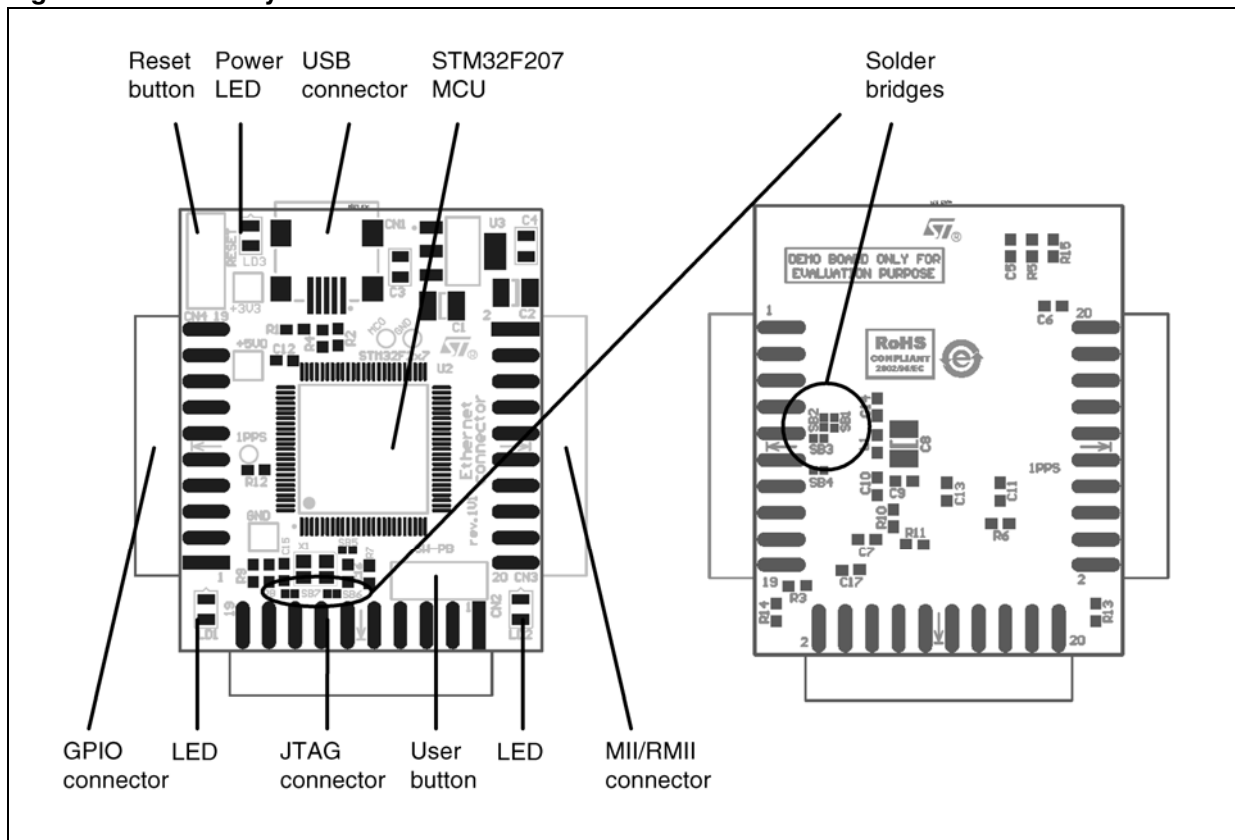
5.1 ST802RT1A Ethernet PHY demonstration board

Figure 8. Board layout - ST802RT1A Ethernet PHY demonstration board



5.2 STM32F207 controller demonstration board

Figure 9. Board layout - STM32F207 controller demonstration board



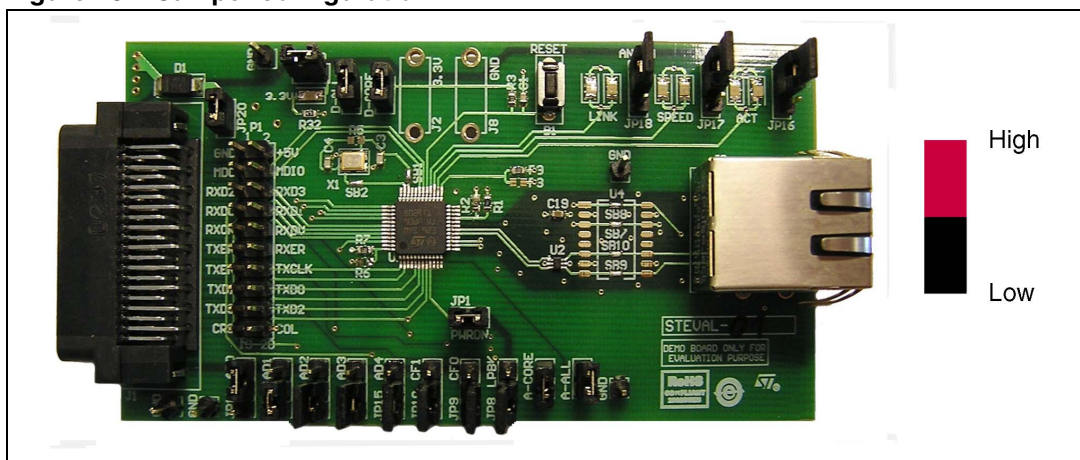
6 Configuration and functionality

This section describes configuration and functionality of the ST802RT1A Ethernet PHY demonstration board and STM32F207 controller demonstration board.

6.1 Configuration and functionality- ST802RT1A Ethernet PHY demonstration board

Please note that in this section jumper configuration “high” means that the jumper is placed in the position closest to the top edge of the board and position “low” means that the jumper is placed in the position closest to the bottom edge of the board, as depicted in [Figure 10](#).

Figure 10. Jumper configuration



6.1.1 BOOT strap options

The ST802RT1A PHY uses many of the functional pins as strap options. The values of these pins are sampled during hardware reset-power-up and are used to strap the device into specific modes of operation. The ST802RT1A provides a simple strap option to automatically configure some device modes with no device register configuration necessary. All strap pins have a weak internal pull-up or pull-down. If the default strap value must be changed, it should not be connected directly to V_{CC} or GND, but an external 2.2 k Ω resistor should be used. The software reset and power-down through the power-down pin cannot be used to change the strap configuration.

Auto-negotiation

Auto-negotiation is performed as part of the initial setup of the link, and allows the PHYs at each end of a cable to advertise their capabilities (speed, PHY type, half or full duplex) and to automatically select the operating mode for communication on the link. If auto-negotiation is disabled, the chip stays at the speed that is selected by the strap pins. If partner speed is the same, the link ON state is signaled otherwise no link state is signaled.

Table 1. Auto-negotiation jumper settings⁽¹⁾

Jumper	Description	Default configuration
JP16	AN_1	High
JP17	AN_0	High
JP18	AN_EN - auto-negotiation enable; when "high" - auto-negotiation enabled, when "low" - auto-negotiation disabled	High

1. See functionality of AN_xxx pins in the ST802RT1 datasheet.

PHY MII address

The MDIO/MDC serial management interface is used to access the internal registers of the PHY. The Ethernet MAC that is connected to the PHY must know the appropriate PHY address for successful communication. A special case is the PHY address 0x00. If this address is used as the bootstrap address during the reset, the 00000 value is latched into the internal receive mode control register RN14 (0x14h) but the PHY goes also to isolation mode. It is possible to change the PHY address by writing the RN14 register later when the application is already running.

Table 2. PHY MII address jumper settings

Jumper	Description	Default configuration
JP11	MII address 0	High
JP12	MII address 1	Low
JP13	MII address 2	Low
JP14	MII address 3	Low
JP15	MII address 4	Low

Power-down

This pin is an active low input of the PHY and should be asserted low to put the device into power-down mode. During power-down mode, TXP/TXN outputs and all LED outputs are 3-stated, and the MII interface is isolated. The power-down functionality is also achievable through software by asserting bit 11 of register RN00.

Table 3. Power-down jumper setting

Jumper	Description	Default configuration
JP1	Power-down, if fitted - PHY works normally; if not fitted - PHY is in power-down mode	Fitted

Loopback

Local loopback passes data internally from the transmitting to the receiving serial analog logic. There are two ways to enter the internal loopback mode, either by writing RN00

register, bit 14 (MDIO/MDC) or by using the boot strap LPBK pin (V_{DD} - enabled, GND - disabled, through 2.2 k Ω resistor).

Table 4. Loopback jumper setting

Jumper	Description	Default configuration
JP8	LPBK - loopback; "high" - internal loopback selected (mainly for debug purposes); "low" - normal operation	Low

MII/RMII mode selection

There is a strapping option available which allows to set the operating mode of the MAC Data Interface. Default operation (no pull-ups) enables normal MII mode of operation. Strapping CF0 high causes the device to be in RMII.

Table 5. MII/RMII jumper settings

Jumper	Description	Default configuration
JP9	CF0 - MAC data interface selection	Low
JP10	CF1 - MAC data interface selection	Low

Table 6. MII/RMII interface selection - logic table

Interface	CF0 (JP9)	CF1 (JP10)
MII	Low	X
RMII	High	Low

6.1.2 Solder bridges

The SB1 and SB2 solder bridges are used to connect 25 MHz crystal X1 to the ST802RT1A PHY in the MII mode of operation. They can be removed in order to disconnect the crystal when an external 25 MHz clock signal comes from the MCO pin of the P1 connector (pin 11). In this case, SB3 solder bridge must be closed to bring the 25 MHz clock signal to the X1 pin of the PHY. In RMII mode, the 25 MHz clock is not used, the PHY is clocked with a 50 MHz clock signal coming to its TXD2 pin.

6.1.3 RESET button

The RESET button resets the ST802RT1A PHY to its initial state.

6.1.4 LEDs

By default, the LEDs have the following functionality:

Table 7. LED functionality - alternative 1

LED	Description	Details
LED1	BLINK for activity	JP16 is low
LED2	BLINK for activity	JP16 is high
LED3	ON for 100 Mb / OFF for 10 Mb	JP17 is low
LED4	ON for 100 Mb / OFF for 10 Mb	JP17 is high
LED5	ON for link up / OFF for link down	JP18 is low
LED6	ON for link up / OFF for link down	JP18 is high

Alternatively, it is possible to change the meaning of LED1 - LED6 by writing the PHY register RN1B [0d27, 0x1B]:

Table 8. LED functionality - alternative 2

LED	Description	Details
LED1	ON for full duplex, BLINK for collision	JP16 is low
LED2	ON for full duplex, BLINK for collision	JP16 is high
LED3	ON for 100 Mb / OFF for 10 Mb	JP17 is low
LED4	ON for 100 Mb / OFF for 10 Mb	JP17 is high
LED5	ON for link up and BLINK for activity / OFF for link down	JP18 is low
LED6	ON for link up and BLINK for activity / OFF for link down	JP18 is high

There is also LED8 on the board, which is used for indicating that the board is powered.

6.1.5 Test point MCO

The test point MCO can be used to connect the external clock signal to the clock input of the ST802RT1A PHY in MII mode. Note that the 25 MHz crystal X1 must be disconnected from the ST802RT1A PHY by removing solder bridges SB1 and SB2 before connecting any external signal to the test point.

6.2 Configuration and functionality - STM32F207 controller demonstration board

6.2.1 MII/RMII configuration

The STM32F207 controller demonstration board can be configured to communicate with Ethernet PHY using either the MII or RMII interface. The configuration is done using three solder bridges SB1, SB2, and SB3.

Table 9. MII/RMII interface selection by solder bridges SB1, SB2, and SB3

Interface	SB1	SB2	SB3
MII	Remove	Remove	Fit
RMII	Fit	Fit	Remove

In MII mode, the ST802RT1A Ethernet PHY demonstration board can be clocked either from its onboard 25 MHz crystal oscillator or by the 25 MHz clock signal output - MCO from the STM32F207 controller demonstration board, see [Section 6.1.5](#) and [6.2.4](#). Both MCO pins (test points) must be interconnected by an additional wire.

In RMII mode, the ST802RT1A Ethernet PHY demonstration board is clocked from the 50 MHz clock signal output delivered from the STM32F207 controller demonstration board.

6.2.2 MCO

In order to set up the board to deliver 25 MHz to the ST802RT1A PHY demonstration board, the onboard solder bridge SB4 must be closed. The 25 MHz clock signal is then externally available through pin 11 of the CN3 connector.

6.2.3 Buttons

There are two buttons on the STM32F207 controller demonstration board. The RESET button resets the STM32F207 MCU to its initial state. The B1 general purpose button is connected to the PA4 pin of the STM32F207 MCU and is active low.

6.2.4 LEDs

There are three LEDs on the STM32F207 controller demonstration board. LD1 and LD2 are general purpose LEDs connected to PC13 and PC14 pins of the STM32F207 MCU. LD3 is used for indicating that the board is powered.

6.2.5 Crystal or oscillator

The board is, by default, equipped with a 25 MHz crystal unit. Nevertheless, the board crystal can be replaced by an oscillator (e.g. SG-310SCB).

Table 10. Crystal and oscillator set-up by solder bridges SB5, SB6, and SB7

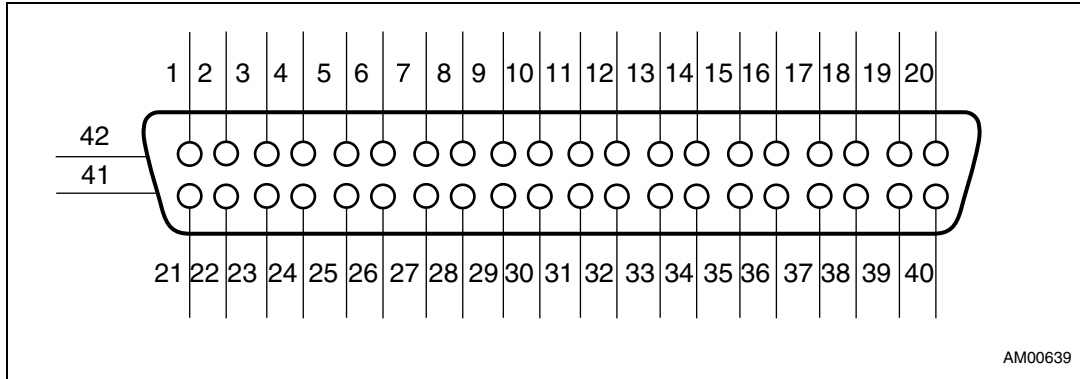
	SB5	SB6	SB7
Crystal (default)	Fit	Fit	Remove
Oscillator	Remove	Remove	Fit

7 Connectors

7.1 Connectors for the ST802RT1A Ethernet PHY demonstration board

7.1.1 MII/RMII debugging connector J1

Figure 11. MII/RMII debugging connector J1



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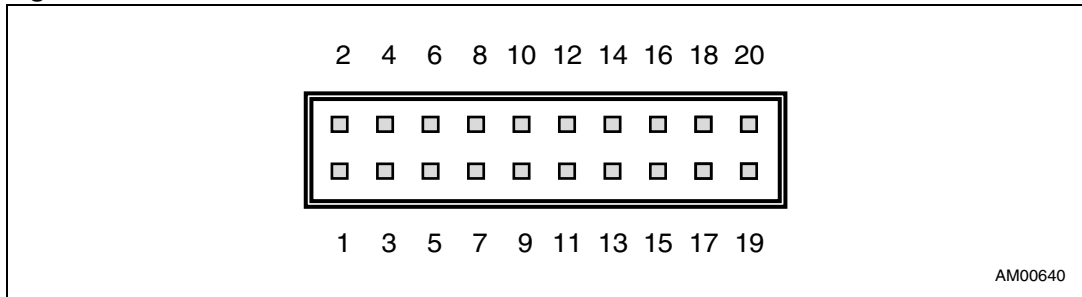
Table 11. MII/RMII debugging connector J1⁽¹⁾

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+5 V	12	TXCLK	23	GND	34	GND
2	MDIO	13	TXEN	24	GND	35	GND
3	MDC	14	TXD_0	25	GND	36	GND
4	RXD_3	15	TXD_1	26	GND	37	GND
5	RXD_2	16	TXD_2	27	GND	38	GND
6	RXD_1	17	TXD_3	28	GND	39	GND
7	RXD_0	18	COL	29	GND	40	Not connected
8	RXDV	19	CRS	30	GND	41	GND
9	RXCLK	20	Not connected	31	GND	42	GND
10	RXER	21	+5 V	32	GND		
11	MCO (25 MHz)	22	GND	33	GND		

1. Pin 11 can be used as 25 MHz system clock input of the PHY.

7.1.2 MII/RMII connector P1

Figure 12. MII/RMII connector P1



AM00640

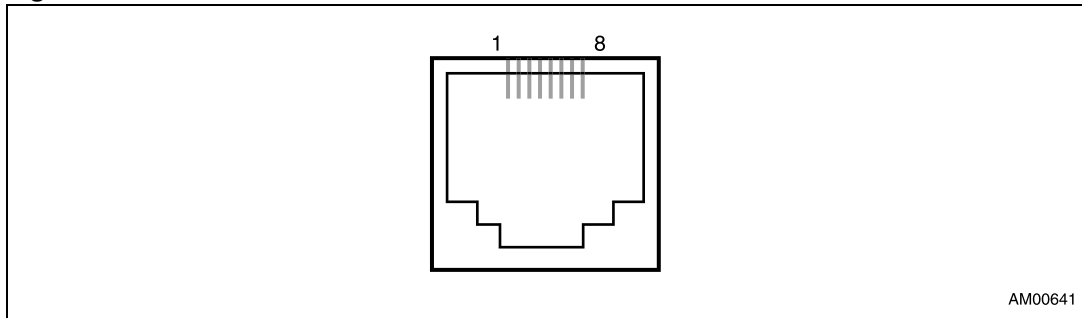
Table 12. MII/RMII connector P1

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	RXD3	11	25 MHz external system clock ⁽¹⁾	16	TXD0
2	+5 V	7	RXD0	12	RXER	17	TXD3
3	MDC	8	RXD1	13	TXEN	18	TXD2
4	MDIO	9	RXCLK	14	TXCLK	19	CRS
5	RXD2	10	RXDV	15	TXD1	20	COL

1. Pin 11 can be used as 25 MHz system clock input of the PHY.

7.1.3 RJ45 connector J9

Figure 13. Ethernet RJ45 connector J9 - front view



AM00641

Table 13. Ethernet RJ45 connector J9

Pin number	Description	Pin number	Description
1	TxData+	2	TxData-
3	RxData+	4	NC
5	NC	6	RxData-
7	NC	8	NC

7.2 Connectors of the STM32F207 controller demonstration board

7.2.1 USB connector CN1

Figure 14. USB connector CN1

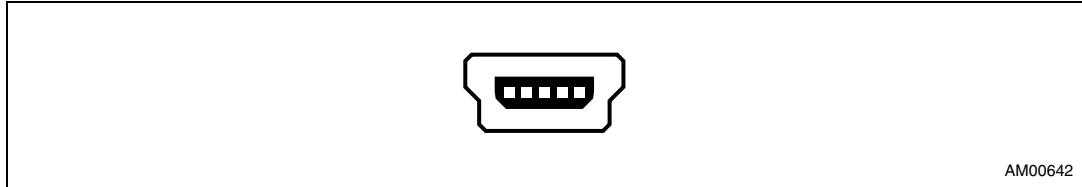


Table 14. USB connector CN1

Pin	Signal	Pin	Signal
1	V _{BUS}	4	ID
2	D-	5	GND
3	D+	6	SH

7.2.2 JTAG connector CN2

The 20-pin connector (CN2) provides the JTAG interface. This interface is primarily used for communicating with a PC using a suitable USB/JTAG converter box such as J-Link from IAR Systems or R-Link from Raisonance, etc. There exists a wide choice of development tools on the market supporting microcontroller Flash memory programming and application debugging.

Figure 15. JTAG connector CN2

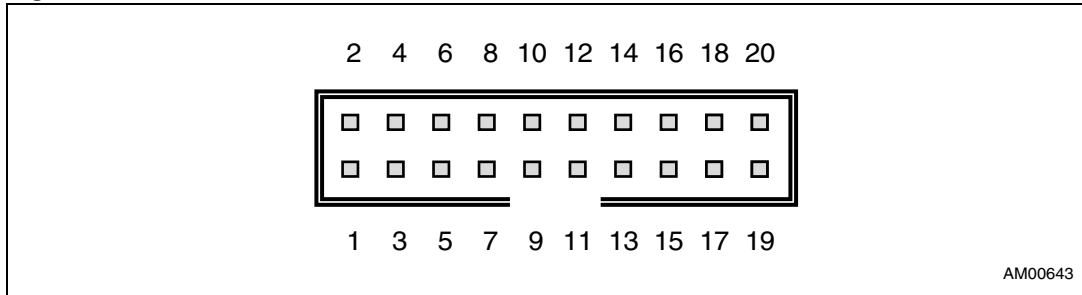
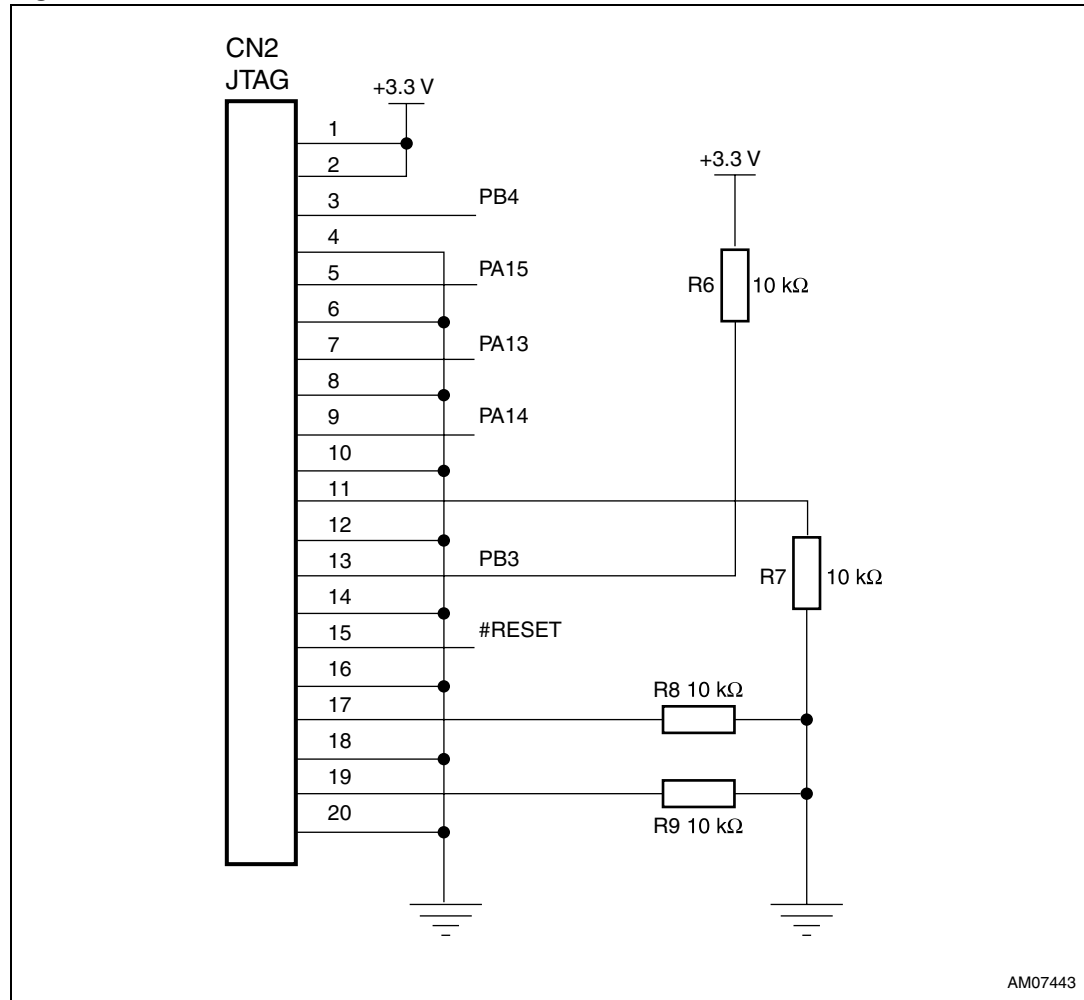


Table 15. JTAG connector CN2

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	3.3 V DC	6	GND	11	RTCK connected to GND by R7 (10 kΩ)	16	GND
2	3.3 V DC	7	JTMS	12	GND	17	DBGQRQ connected to GND by R8 (10 kΩ)
3	JTRST	8	GND	13	JTDO connected to 3.3 V DC by R6 (10 kΩ)	18	GND
4	GND	9	JTCK	14	GND	19	DBGACK connected to GND by R9 (10 kΩ)
5	JTDI	10	GND	15	NRST	20	GND

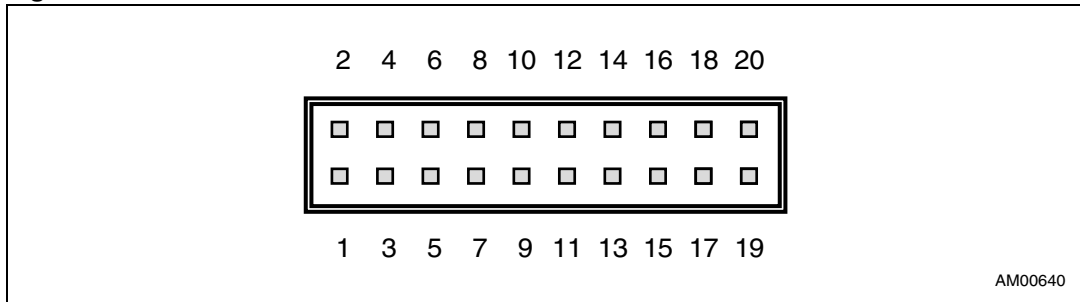
Figure 16. JTAG connector CN2 – schematic



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7.2.3 MII/RMII connector CN3

Figure 17. MII/RMII connector CN3



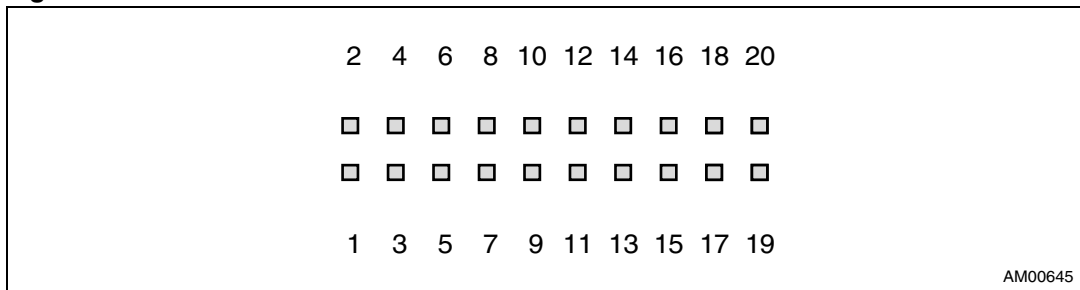
AM00640

Table 16. MII/RMII connector CN3

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	RXD3	11	MCO (25 MHz)	16	TXD0
2	+5 V	7	RXD0	12	RXER	17	TXD3
3	MDC	8	RXD1	13	TXEN	18	TXD2
4	MDIO	9	RXCLK	14	TXCLK	19	CRS
5	RXD2	10	RXDV	15	TXD1	20	COL

7.2.4 GPIO connector CN4

Figure 18. GPIO connector CN4



AM00645

Table 17. GPIO connector CN4

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	PD3	11	PD4	16	PE0
2	+5 V	7	+3.3 V	12	PC12	17	PD7
3	PA6	8	PA15	13	PD5	18	PE1
4	PD2	9	GND	14	PC7	19	GND
5	PA5	10	PC10	15	PD6	20	+3.3 V

Appendix A ST802RT1A Ethernet PHY demonstration board - BOM list

Table 18. ST802RT1A - BOM list

Designator	Quantity	Description	Value	Order	Not assembled
B1	1	Pushbutton (DT2112C)	RESET	GM Electronic®: 630-121 Farnell: 9471898	
C1, C2	2	Generic capacitor	10 nF	Farnell: 1709948	
C3, C4	2	Generic capacitor	12 pF	Farnell: 1462447	
C5, C6, C7, C9, C10, C11, C14, C15, C17, C18, C19	11	Generic capacitor	100 nF	Farnell: 4532004	C10, C17
C8, C12	2	Generic capacitor	1 µF / X5R Murata GRM188R60J105KA01	Murata Manufacturing Co., Ltd.: GRM188R60J105KA01 Farnell: 1710296	
C13, C16	2	Generic polarized capacitor	10 µF / tantalum	Farnell: 1213794	
D1	1	Schottky diode	STPS160A / STPS2L40U	STMicroelectronics™: STPS2L40U	
J1	1	Plug assembly, 40-pin connector	Connector 40	Tyco Electronics: 174218-2; Fujitsu: FCN-238P040-G/F	J1
J2, J8	2	1-pin header, 2 mm Banana Receptacle	2MM_REC		J2, J8
J3, J4, J5, J6, J7	5	1-pin header	GND	Farnell: 1593411	
J9	1	RJ45 Ethernet connector with integrated magnetic	RJ-45	Pulse Electronics: J00-0086NL	
JP1, JP4, JP5, JP6, JP7, JP19, JP20	7	2-pin jumper wire	Jumper	Farnell: 1593411	
JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18	11	3-pin jumper wire	Jumper3	Farnell: 1593412	
L1, L2	2	Ferrite bead	NFE31PT222Z1E9L Murata	Farnell: 9528172	
LED1, LED2	2	Generic LED	Yellow	Farnell: 1226420	

Table 18. ST802RT1A - BOM list (continued)

Designator	Quantity	Description	Value	Order	Not assembled
LED3, LED4, LED8	3	Generic LED	Red	Farnell: 1226392	
LED5, LED6	2	Generic LED	Green	Farnell: 1226373	
P1	1	Header, 20-pin, dual row	Header 10 x 2	Farnell: 1593446	
R1	1	Generic resistor	5.6 K Ω	Farnell: 1514773	
R2	1	Generic resistor	91 K Ω	Farnell: 1646361	
R3, R4	2	Generic resistor	10 K Ω	Farnell: 1601277	
R5	1	Generic resistor	1 M Ω N.A.	Farnell: 1631320	R5
R6, R8	2	Generic resistor	750 Ω	Farnell: 1399909	R6, R8
R7, R9	2	Generic resistor	1.2 K Ω	Farnell: 1632396	
R17, R18, R19, R20, R21, R22, R23, R24	8	Generic resistor	2.2 K Ω	Farnell: 1632417	
R25	1	Generic resistor	330 Ω	Farnell: 1646224	
R26, R28, R30	3	Generic resistor	2 K Ω	Farnell: 1632414	
R27, R32	2	Generic resistor	470 Ω	Farnell: 9367659	
R29	1	Generic resistor	220 Ω	Farnell: 1646159	
R31, R33, R34, R35	4	Generic resistor	75 Ω	Farnell: 9331549	R31, R33, R34, R35
SB1, SB2, SB3, SB4, SB5, SB6, SB7, SB8, SB9, SB10	10	Soldering bridge	Solder bridge		SB3, SB4, SB5
U1	1	10/100 Fast Ethernet 3.3 V transceiver	ST802RT1A	ST: ST802RT1A	
U2, U5	2	ESD protection, DALC208SC6	DVIULC6-2P6	ST: DVIULC6-2P6	
U3	1		LD1117S33	ST: LD1117S33	
U4	1	H1300 Ethernet transformer	H1300 (Pulse)		
X1	1	Epson Crystal: FA-238	25 MHz	Farnell: 1712818	

Appendix B Appendix B STM32F207 controller demonstration board - BOM list

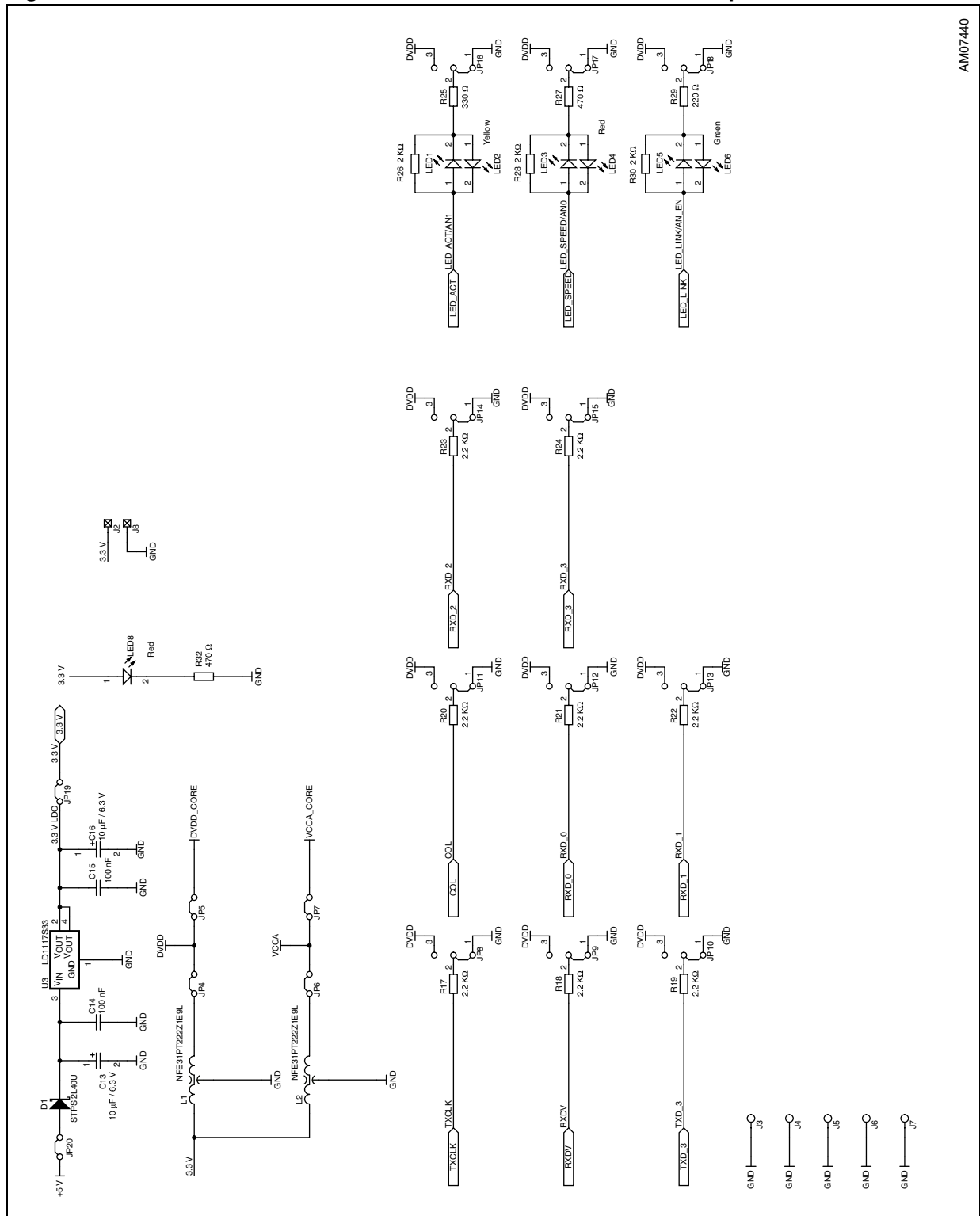
Table 19. STM32F207- BOM list

Designator	Quantity	Description	Value	Order	Not assembled
C1, C2, C8	3	Polarized capacitor (surface mounted)	10 μ F / 6.3 V	Farnell: 1213794	
C3, C4	2	Capacitor	100n_0805	Farnell: 1414664	
C6, C17	2	Capacitor	100nF_0603	Farnell: 4532004	
C5, C7, C9, C10, C11, C12, C13, C14	8	Capacitor	10 nF	Farnell: 1709948	
C15, C16	2	Capacitor	12 pF	Farnell: 1462447	
CN1	1	MOLEX - 675031020 - socket, USB, mini-B, SMT, W/PEGS	USB_1X90A	Farnell: 1125348	
CN2	1	Header, 20-pin, dual row, with key	JTAG	Farnell: 1099258	
CN3	1	Socket, 20-pin, dual row, side mounting	Socket 10 x 2, BL820GD	Farnell: 1593494 GM Electronic: 832-009	
CN4	1	Socket, 20-pin, dual row, side mounting	Socket 10 x 2, BL820GD	Farnell: 1593494 GM Electronic: 832-009	
L1	1	Inductor, 'BLM18BA05OSN1D	BEAD	Farnell: 1515680	
LD1	1	Typical red, green, yellow, amber GaAs LED	Yellow	Farnell: 1226420	
LD2	1	Typical red, green, yellow, amber GaAs LED	Green	Farnell: 1226373	
LD3	1	Typical red, green, yellow, amber GaAs LED	Red	Farnell: 1226392	
R1	1	Resistor	1k5_0603	Farnell: 1632406	
R2, R4	2	Resistor	22R_0603	Farnell: 1692521	
R3, R6, R7, R8, R9, R12	6	Resistor	10k_0603	Farnell: 1601277	
R5	1	Resistor	1M_0603	Farnell: 1631320	R5
R10	1	Resistor	47R_0603	Farnell: 1646283	
R11	1	Resistor	0R_0603	Farnell: 1573911	

Table 19. STM32F207- BOM list

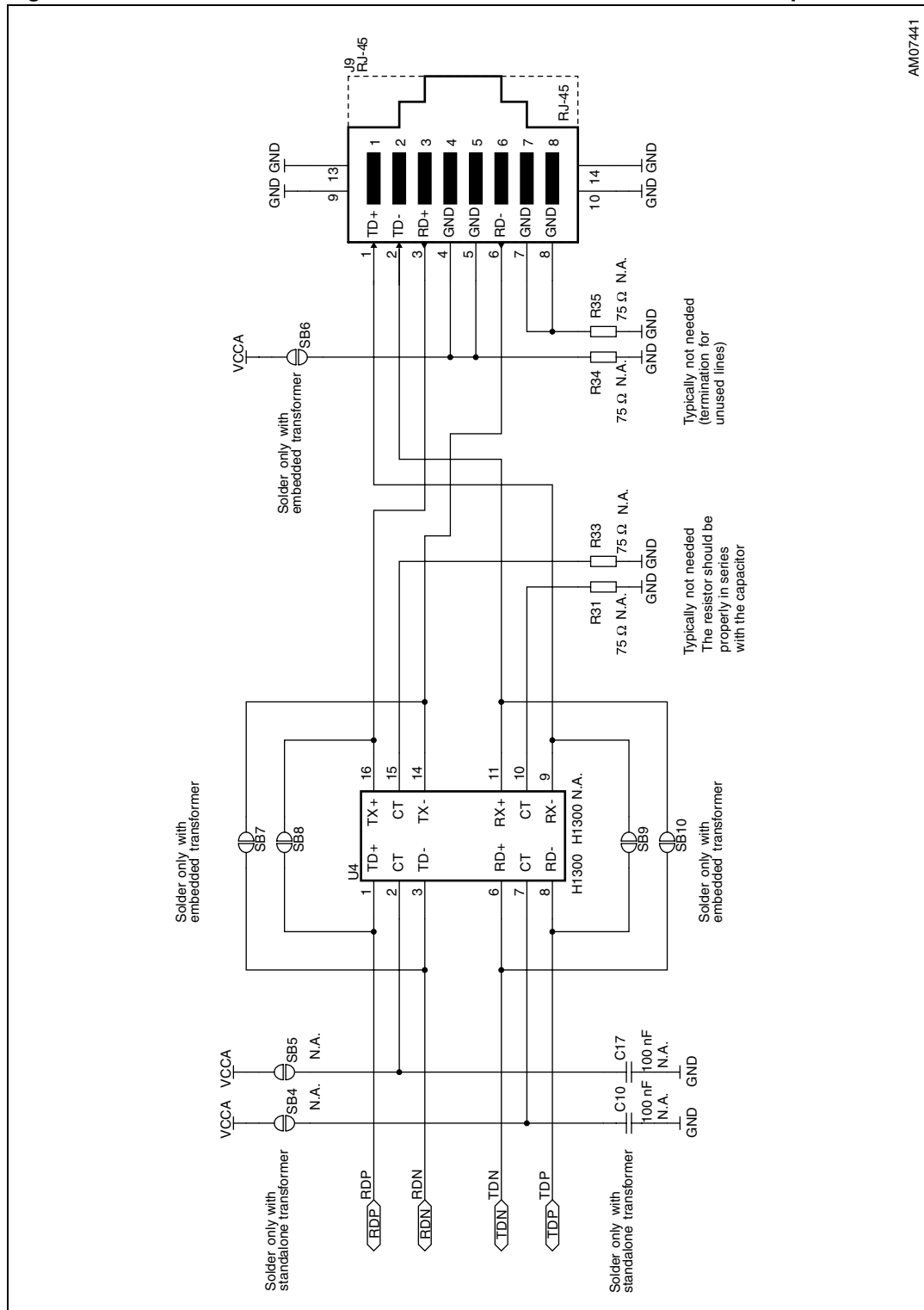
Designator	Quantity	Description	Value	Order	Not assembled
R13	1	Resistor	330 Ω	Farnell: 1646224	
R15	1	Resistor	470 Ω	Farnell: 9367659	
R14	1	Resistor	220 Ω	Farnell: 1646159	
RESET1	1	Switch	Reset	GM Electronic: 630-121 Farnell: 9471898	
RESET2	1	Switch	B1	GM Electronic: 630-121 Farnell: 9471898	
U2	1	MCU	STM32F207	ST: STM32F207VGT6	
U3	1	Low drop voltage regulator	LD1117S33	ST: LD1117S33	
X1	1	Epson Crystal: FA-238	25 MHz	Farnell: 1712818	
SB1, SB2, SB3, SB4, SB5, SB6, SB7	7	Solder bridge			SB1, SB2, SB7

Figure 20. ST802RT1A Ethernet PHY demonstration board - schematic part 2



AM07440

Figure 21. ST802RT1A Ethernet PHY demonstration board - schematic part 3



AM07441

Revision history

Table 20. Document revision history

Date	Revision	Changes
28-Jan-2011	1	Initial release.

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